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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 06/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/802,522	SUKHAREV ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/17/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: please add the information of the parent case 10/448,082 (now US. PAT. 6,777,807) at the beginning of the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-2, 4-7, 9-10, and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Lopatin et al. (US Pat. No. 6,528,409 B1).

Regarding claim 1, Lopatin et al. teaches a method of forming a metal interconnect in an integrated circuit, the method comprising the steps of:

forming a copper layer (230) over dielectric structures (consider the structure comprising dielectric layers 222 and 224) on the integrated circuit, where the dielectric structures have an upper level [see fig. 8];

planarizing the copper layer (230) to be no higher than the upper level of the dielectric structures, without reducing the upper level of the dielectric structures (consider the dielectric layer 224 as the upper level) [see fig. 9]; and

forming an electrically conductive capping layer (234) over all of the copper layer (234), without the capping layer forming over any of the dielectric structures (please note that the capping layer 234 is formed only on the copper layer 230) [see fig. 12].

Regarding claim 2, Lopatin et al. further teaches the step of forming the copper layer (230) comprises forming the copper layer using electrochemical deposition [col. 1, lines 53-54: Lopatin teaches that the copper is typically formed by electroplating process].

Regarding claim 4, Lopatin et al. further teaches that the step of forming the electrically conductive capping layer (234) comprises electroless deposition of the electrically conductive capping layer [col. 9, lines 56-57].

Regarding claim 5, Lopatin et al. further teaches that the dielectric structures comprise low k materials (222) [col. 7, lines 18-19].

Regarding claim 6, Lopatin et al. further teaches that the electrically conductive capping layer comprises cobalt [col. 9, lines 50-56].

Regarding claim 7, Lopatin et al. further teaches that the electrically conductive capping layer (please consider layer 232 as the capping layer instead of layer 234) [see fig. 10 and col. 9, lines 2-4].

Regarding claims 9-10 and 18, Lopatin et al. teaches an integrated circuit, the improvement comprising a metal interconnect including:

a copper layer (230) formed between dielectric structures (consider the structure comprises of dielectric layers 222 and 224), where the dielectric structures have an upper level (consider the exposed upper surface of dielectric 224), where the upper level of the dielectric structures is substantially uniform across all of the dielectric structures (consider the uniform upper surface of dielectric 224) [see fig. 9],

the copper layer (230) planarized to be no higher than the upper level of the dielectric structures (please note that the upper surface of the planarized copper layer 230 is coplanar with the exposed upper surface of dielectric layer 224), the copper layer having no dishing between the dielectric structures (please note that the upper surface of the planarized copper layer 230 is uniform and smooth indicating that no dishing is formed on the upper surface) [see fig. 9], and

an electrically conductive capping layer (234) over all of the copper layer, with none of the capping layer over any of the dielectric structures (consider the structure comprising dielectric layers 222 and 224) [see fig. 12].

Regarding claim 19, Lopatin et al. further teaches that the capping layer (234) is at least partially above the upper level of the dielectric structures (compare the upper surface of layer 234 with the upper surface of layer 224) [see fig. 12].

Regarding claim 20, Lopatin et al. further teaches that the electrically conductive capping layer (234) comprises an alloy of at least one of cobalt and nickel [see col. 9, lines 49-54].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin et al. (US Pat. No. 6,528,409 B1) in view of Ueno et al. (US 2004/0126548 A1).

Regarding claim 8, Lopatin et al. fails to teach the step of forming an inter metallic dielectric layer over the electrically conductive capping layer and the dielectric structures. However, Ueno et al. teaches that it is well known in the art to form an inter metallic dielectric layer (13) over the electrically conductive capping layer (29) and the dielectric structures (13) [see fig. 4].

Lopatin et al. and Ueno et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have

been obvious to a person of ordinary skill in the art to form an inter metallic dielectric layer over the electrically conductive capping layer and the dielectric structures. The motivation for doing so is increasing the density of integrated circuit structures. Therefore, it would have been obvious to combine Ueno et al. with Lopatin et al. to obtain the invention of claim 8.

7. Claims 3, 11-14 and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin et al. (US Pat. No. 6,528,409 B1) in view of Tsai et al. (US Pat. No. 6,537,144 B1).

Regarding claims 3 and 11, Lopatin et al. a method of forming a metal interconnect in an integrated circuit the method comprising the steps of:

forming a copper layer (230) over dielectric structures (consider the structure comprising dielectric layers 222 and 224) on the integrated circuit, where the dielectric structures have an upper level [see fig. 8], the copper layer formed using electrochemical deposition [col. 1, lines 53-54: Lopatin teaches that the copper is typically formed by electroplating process].;

planarizing the copper layer (230) to be no higher than the upper level of the dielectric structures, without reducing the upper level of the dielectric structures (consider the dielectric layer 224 as the upper level) [see fig. 9]; and

forming an electrically conductive capping layer (234) over all of the copper layer (234), without the capping layer forming over any of the dielectric structures (please note that the capping layer 234 is formed only on the copper layer 230) [see fig. 12], the

electrically conductive capping layer formed using electroless deposition [col. 9, lines 55-57].

However, Lopatin et al. fails to teach that the copper layer is planarized by using electrochemical polishing.

Tsai et al. teaches that it is well known in the art to planarize copper materials by using a polishing step comprising a material that balances electrochemical forces (abstract).

Lopatin et al. and Tsai et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to planarize the copper layer by using a electrochemical polishing process consisting of introducing a material that balances electrochemical forces. The motivation for doing so, as is taught by Tsai et al., is to reduce dishing [abstract]. Therefore, it would have been obvious to combine Tsai et al. with Lopatin et al. to obtain the invention of claims 3, 11-14 and 16-17.

Regarding claim 12, Lopatin et al. further teaches that the dielectric structures comprise low k materials (222) [col. 7, lines 18-19].

Regarding claim 13, Lopatin et al. further teaches that the electrically conductive capping layer comprises cobalt [col. 9, lines 50-56].

Regarding claim 14, Lopatin et al. further teaches that the electrically conductive capping layer (please consider layer 232 as the capping layer instead of layer 234) [see fig. 10 and col. 9, lines 2-4].

Regarding claims 16 and 17, Lopatin et al. teaches the claimed device as stated

before in the rejection of claims 9-10 and 18.

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lopatin et al. (US Pat. No. 6,528,409 B1) in view of Tsai et al. (US Pat. No. 6,537,144 B1), and further in view of Ueno et al. (US 2004/0126548 A1).

Regarding claim 15, a further difference between the prior art and the claimed invention is the step of forming an inter metallic dielectric layer over the electrically conductive capping layer and the dielectric structures. However, Ueno et al. teaches that it is well known in the art to form an inter metallic dielectric layer (13) over the electrically conductive capping layer (29) and the dielectric structures (13) [see fig. 4].

Lopatin et al., Tsai et al. and Ueno et al. are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to further form an inter metallic dielectric layer over the electrically conductive capping layer and the dielectric structures. The motivation for further doing so is increasing the density of integrated circuit structures. Therefore, it would have been obvious to further combine Ueno et al. with Lopatin et al. and Tsai et al. to obtain the invention of claim 15.

Double Patenting

8. A rejection based on double patenting of the "same invention" type finds its support in the language of 35 U.S.C. 101 which states that "whoever invents or discovers any new and useful process ... may obtain a patent therefor ..." (Emphasis added). Thus, the term "same invention," in this context, means an invention drawn to identical subject matter. See *Miller v. Eagle Mfg. Co.*, 151 U.S. 186 (1894); *In re*

Ockert, 245 F.2d 467, 114 USPQ 330 (CCPA 1957); and *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970).

A statutory type (35 U.S.C. 101) double patenting rejection can be overcome by canceling or amending the conflicting claims so they are no longer coextensive in scope. The filing of a terminal disclaimer cannot overcome a double patenting rejection based upon 35 U.S.C. 101.

9. Claims 11-17 are rejected under 35 U.S.C. 101 as claiming the same invention as that of claims 9-15 of prior U.S. Patent No. 6,777,807 B1. This is a double patenting rejection.

Regarding claim 11, claim 9 of US Patent 6,777,807 B1 teaches a method of forming a metal interconnect in an integrated circuit the method [col. 6, lines 11-12] comprising the steps of:

forming a copper layer over dielectric structures on the integrated circuit, where the dielectric structures have an upper level, the copper layer formed using electrochemical deposition [col. 6, lines 13-17];

planarizing the copper layer to be no higher than the upper level of the dielectric structures, without reducing the upper level of the dielectric structures, the copper layer planarized using electrochemical polishing [col. 6, lines 17-21]; and

forming an electrically conductive capping layer over all of the copper layer, without the capping layer forming over any of the dielectric structures, the electrically conductive capping layer formed using electroless deposition [col. 6, lines 22-27].

Regarding claim 12, claim 10 of US Patent 6,777,807 B1 further teaches that the dielectric structures comprise low k materials [col. 6, lines 27-29].

Regarding claim 13, claim 11 of US Patent 6,777,807 B1 further teaches that the

electrically conductive capping layer comprises cobalt [col. 6, lines 30-31].

Regarding claim 14, claim 12 of US Patent 6,777,807 B1 further teaches that the electrically conductive capping layer comprises nickel [col. 6, lines 32-33].

Regarding claim 15, claim 13 of US Patent 6,777,807 B1 further teaches the step of forming an inter metallic dielectric layer over the electrically conductive capping layer and the dielectric structures [col. 6, lines 34-37].

Regarding claim 16, claim 14 of US Patent 6,777,807 B1 further teaches a metal interconnect formed according to the method of claim 11 [col. 6, lines 38-39].

Regarding claim 17, claim 15 of US Patent 6,777,807 B1 further teaches an integrated circuit having a metal interconnect formed according to the method of claim 11 [col. 6, lines 39-41].

10. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

11. Claims 1-10 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-8 of U.S. Patent No.

6,777,807 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because U.S. Patent No. 6,777,807 B1 claims the recited limitations. For instance,

Regarding claim 1, claim 1 of US Patent 6,777,807 B1 teaches a method of forming a metal interconnect in an integrated circuit [col. 5, lines 21-22], the method comprising the steps of:

forming a copper layer over dielectric structures on the integrated circuit, where the dielectric structures have an upper level [col. 5, lines 23-25];

planarizing the copper layer to be no higher than the upper level of the dielectric structures, without reducing the upper level of the dielectric structures [col. 5, lines 26-28]; and

forming an electrically conductive capping layer over all of the copper layer, without the capping layer forming over any of the dielectric structures [col. 5, lines 30-33].

Regarding claim 2, claim 2 of US Patent 6,777,807 B1 further teaches that the step of forming the copper layer comprises forming the copper layer using electrochemical deposition [col. 5, lines 35-37].

Regarding claim 3, claim 3 of US Patent 6,777,807 B1 further teaches that the step of planarizing the copper layer comprises electrochemical polishing of the copper layer [col. 5, lines 38-40].

Regarding claim 4, claim 4 of US Patent 6,777,807 B1 further teaches that the step of forming the electrically conductive capping layer comprises electroless

deposition of the electrically conductive capping layer [col. 5, lines 41-43].

Regarding claim 5, claim 5 of US Patent 6,777,807 B1 further teaches that the dielectric structures comprise low k materials [col. 6, lines 1-2].

Regarding claim 6, claim 1 of US Patent 6,777,807 B1 further teaches that the electrically conductive capping layer comprises cobalt [col. 5, lines 33-34].

Regarding claim 7, claim 1 of US Patent 6,777,807 B1 further teaches that the electrically conductive capping layer comprises nickel [col. 5, lines 33-34].

Regarding claim 8, claim 6 of US Patent 6,777,807 B1 further teaches that the step of forming an inter metallic dielectric layer over the electrically conductive capping layer and the dielectric structures [col. 6, lines 3-6].

Regarding claim 9, claim 7 of US Patent 6,777,807 B1 further teaches a metal interconnect formed according to the method of claim 1 [col. 6, lines 7-8].

Regarding claim 10, claim 8 of US Patent 6,777,807 B1 further teaches an integrated circuit having a metal interconnect formed according to the method of claim 1 [col. 6, lines 9-10].

Conclusion

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Whitehair et al. (US 2003/0001240 A1) teaches a flat planarized copper structure (131) with a Nickel capping layer (132) formed on it (fig. 2B); Catabay et al. (US Pat. No. 6,881,664 B2) is related to the present application and teaches a well

known electrochemical polishing process (abstract); and Chan et al. (US Pat. No. 6,214,728 B1) teaches a copper plug with a capping layer (14) (abstract);

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

José R. Díaz
Examiner
Art Unit 2815